

### **REMARKS**

Reconsideration is requested.

Claims 30-39 are in the application for consideration.

Claims 30-31, 36-37, and 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gonzalez (U.S. Patent No. 5,693,971) in view of Potter (U.S. Patent No. 5,901,078). Claims 32-35, and 37 stand objected as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including the limitations of the base claim and any intervening claims.

The title has been amended to be consistent with the claimed subject matter. Portions of the specification have been amended to correct minor typographical errors. No new matter is being introduced by way of this amendment.

The rejection of claims 30-31, 36-37, and 39 is respectfully traversed.

Claim 30 recites, in part, forming the isolation gate includes forming the isolation gate to have a second threshold voltage greater than the first threshold voltage.

The Office Action alleges that Potter at col. 1, lines 24-40 and col. 2, lines 1-25 teaches the above recited feature of claim 30 and asserts that Potter shows "that during normal operations of the DRAM devices the isolation gates have a threshold voltage greater than the threshold voltage of the first and second access transistors." The Examiner is mistaken.

Potter's col. 1, lines 24-40 discloses "in normal operation, the isolation gates (are) selectively turned on and off during read, sense and restore cycles...As  $V_{cc}$  decreases, the threshold voltage of the isolation gates becomes relatively large and affects the ability of the sense amplifiers to sense the charge stored on the cells. Further, high  $V_t$  relative to  $V_{cc}$  can affect the ability to restore the sensed cell due to significant resistance presented by the isolation gate." (Emphasis Added)

Further, Potter's col. 2, lines 1-25 disclose three different scenarios related to isolation gate voltage. In the first, the voltage on the isolation gate is increased greater than  $V_t$ . In the second, the voltage on the isolation gate is increased to  $V_{ccp}$  both during access time and during restore time. In the third, the voltage on the isolation gate is held at  $V_{cc}$  for both access and sense cycles.

The above disclosure of Potter merely illustrates a relationship between isolation gate voltage and  $V_{cc}$  for speeding the driving of the sense amplifier lines to  $V_{cc}$  and ground. See, for example, Potter's col. 1, lines 60-65 which discloses "during restore time, the isolation gate voltage is again raised above the supply voltage to minimize the effects of isolation transistor threshold voltage." (Emphasis Added) There is no suggestion, whatsoever, in Potter, regarding a relationship between the threshold voltage of the isolation gate and a threshold voltage of a first and second transistors.

In view of the above, Potter fails to teach or suggest that the isolation gate is formed to have a second threshold voltage that is greater than the first threshold voltage (of the first and second transistors). The paragraph bridging

pages 14 and 15 of the present specification provides further details for having increased threshold voltage associated with the isolation gate.

Accordingly, even if the teachings of Potter are combined with those of Gonzalez, all the elements of claim 30 are not met. Claim 30 is therefore allowable.

As claims 31, 36, 37, and 39 depend on claim 30, they too are allowable.

It is believed that this application is in condition for immediate allowance, and action to that end is respectfully requested.

The undersigned is available for telephone consultation at any time if such would facilitate prosecution of this application.

Respectfully submitted,

Dated: April 19, 2004

By: K. Satheesh Karra  
Satheesh Karra  
Reg. No. 40,246